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EXAMINER
HERNANDEZ, WILLIAM

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BINLING ZHOU and JAMES L. TODSEN

Appeal 2008-5547
Application 10/779,903
Technology Center 2800

Decided:[1] February 6, 2009

Before JOSEPH F. RUGGIERO, JOHN A. JEFFERY,
and R. EUGENE VARNDELL, JR., *Administrative Patent Judges*.

VARNDELL, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 2-23, 25, and 26 under 35 U.S.C. § 103(a). We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

The invention claimed on appeal is directed to an integrator circuit, a CT (computed tomography) scanner data operation system comprising the integrator circuit, and a method of operating the scanner data operation system (Spec. 1, 7, 8). The integrator circuit (30) includes an input conductor for conducting an input current (Iin), an amplifier stage having an input coupled to the input conductor, an integrating capacitor (Cint) coupled between the input of the amplifier stage and an output of the amplifier stage, and an MOS capacitor 20 coupled between an output 14 of the amplifier stage 13 and a voltage conductor for biasing the MOS capacitor (Spec. 7, Fig. 3).

Claim 2, which further illustrates and represents the invention claimed on appeal, follows:

> 2. An integrator circuit comprising:
>
> (a) an input conductor for conducting an input current;
>
> (b) a first amplifier stage having an input coupled to the input conductor;
>
> (c) a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage;
>
> (d) an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage; and
>
> (e) an MOS compensation capacitor coupled between the input and output of the second amplifier stage.

The Examiner relies on the following prior art to show unpatentability:

Prior Art Figs. 1 and 2 of the present application.		
Rapp	US 5,280,420	Jan. 18, 1994
Verhaeghe	US 5,479,132	Dec. 26, 1995
Jung	US 2005/0127885 A1	Jun. 16, 2005

The Final Rejection mailed on July 7, 2006 set forth a rejection of all pending claims 1-26 as being unpatentable under 35 U.S.C. § 103(a) over Prior Art Figs. 1 and 2 of the present application in view of Verhaeghe, Rapp, or Jung. An Amendment After Final filed on December 11, 2006, which was entered by the Examiner, canceled claims 1 and 24. Accordingly, claims 2-23, 25, and 26 are on appeal.

Appellants filed an Appeal Brief on December 11, 2006. The Examiner mailed an Answer on April 10, 2007. Appellants only argue the patentability of the use or arrangement of the MOS compensation capacitor in independent claim 2, which is also defined in independent claims 12, 25, and 26 on appeal (Br. 6-8). Appellants' Brief contains no separate arguments for claims 3-11and 13-23. Arguments which Appellants could have made but did not make in their Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii). Therefore, all claims on appeal stand or fall with independent claim 2.

ISSUE

The Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute one well-

known capacitor, such as that shown by Verhaeghe, Rapp, or Jung, for the capacitor used in circuits of Prior Art Figs. 1 and 2 of the present application (Ans. 4-5). Appellants argue that it would not have been obvious to substitute the MOS compensation capacitor of Verhaeghe, Rapp, or Jung for the polysilicon capacitor in Appellants' Prior Art Figs. 1 and 2 (Br. 6-7).

From the above contentions of Appellants and the Examiner, we frame the issue on appeal as:

> Have Appellants shown that the Examiner erred by finding that one of ordinary skill in the art would have found it obvious to substitute the well-known MOS compensation capacitor, such as taught by Verhaeghe, Rapp, or Jung, for the polysilicon capacitor used in circuits of Prior Art Figs. 1 and 2?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. The integrator circuit shown in Prior Art Figs. 1 and 2 of the present application teaches all elements of the integrator circuit set forth in claim 2 on appeal with one exception. The integrator circuit of Prior Art Figs. 1 and 2 includes a polysilicon capacitor (20) coupled between the input and output of the second amplifier stage, whereas claim 2 on appeal requires an MOS compensation capacitor (20) between the input and output of the second amplifier stage (Spec. 2-8, Figs. 1-2).

2. Fig. 4A of Verhaeghe shows a circuit including common capacitors 40 and 42. Figs. 4B and 4C of Verhaeghe are well-known diagrams of capacitor-connected MOS transistors and show replacing the

common capacitors in Fig. 4A with capacitor-connected MOS transistors (col. 2, ll. 52-57; col. 3, ll. 14-26).

3. Rapp and Jung teach that MOS transistors are more efficiently implemented in silicon than capacitors and diodes with unconstrained terminals (Rapp, col. 7, ll. 10-16; Jung, Fig. 3).

4. It is well-known in the art that MOS capacitors occupy a smaller area than polysilicon capacitors. See, for example, U.S. Patent No. 5,544,102 of Tobita at column 7, lines 44-49.

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. §103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

Discussing the question of obviousness of a patent that claims a rearrangement of known elements, the Court in *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740 (2007) explained:

> If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

The court also explained that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant

field to combine the elements in the way the claimed new invention does." 127 S. Ct. at 1741.

ANALYSIS

Appellants establish no error in the Examiner's conclusion of obviousness. Appellants argue that Prior Art Fig. 2 does not suggest a MOS capacitor (Br. 6). However, the Examiner never found that Prior Art Fig. 2 teaches a MOS capacitor (FF 1), nor is this necessary to support the Examiner's rejection. The integrator circuit of Prior Art Figs. 1 and 2 teaches all elements of the integrator circuit set forth in claim 2 on appeal with the exception of an MOS compensation capacitor arranged between the input and output of the second amplifier stage (FF 1). MOS compensation capacitors are well known in the art (FF 2-4). Accordingly, the Examiner established that all elements in claim 2 on appeal are known in the art, and Appellants establish no error in these facts.

Appellants argue that the MOS capacitors of Verhaeghe, Rapp, or Jung are arranged or used differently than required in claim 2 on appeal (Br. 7). Assuming this argument is correct; it does not establish error in the Examiner's conclusion of obviousness. The Examiner established that common capacitors and capacitor-connected MOS transistors are functionally equivalent (FF 2), which supports the conclusion that it would have been obvious to substitute one well-known capacitor for another. The Examiner further established reasons for substituting capacitor-connected MOS transistors for common capacitors, which include that capacitor-connected transistors are more efficiently implemented in silicon than capacitors and diodes with unconstrained terminals (FF 2-3) and it is well-

known that capacitor-connected MOS transistors occupy a smaller area than polysilicon capacitors (FF 4). Appellants establish no error in these facts or reasons set forth by the Examiner.

For these reasons, Appellants establish no error in the Examiner's conclusion of obviousness of claim 2 on appeal. Since Appellants have not separately argued the patentability of claims 3-23, 25, and 26, these claims fall with claim 2. Accordingly, the rejection of claims 2-23, 25, and 26 under 35 U.S.C. § 103(a) is affirmed.

ORDER

The Examiner's decision rejecting claims 2-23, 25, and 26 as being unpatentable under 35 U.S.C. § 103(a) over Prior Art Figs. 1 and 2 of the present application in view of Verhaeghe, Rapp, or Jung is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

KIS

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